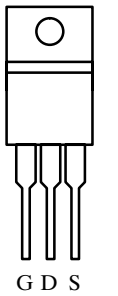
SMP60N03-10L

N-Channel Enhancement-Mode Transistor, Logic Level

Product Summary

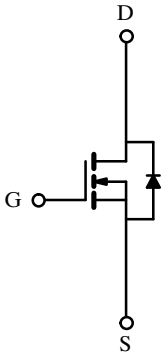
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.01	60

TO-220AB



DRAIN connected to TAB

Top View



N-Channel MOSFET

Absolute Maximum Ratings (T_C = 25°C Unless Otherwise Noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	± 20	
Continuous Drain Current	T_C = 25°C	I_D	60	A
	T_C = 100°C		51	
Pulsed Drain Current		I_{DM}	240	
Avalanche Current		I_{AR}	60	
Avalanche Energy	L = 0.1 mH	E_{AS}	180	mJ
Repetitive Avalanche Energy[a]	L = 0.05 mH	E_{AR}	90	
Power Dissipation	T_C = 25°C	P_D	105	W
	T_C = 100°C		42	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	−55 to 150	°C
Lead Temperature ($^1/_{16}$" from case for 10 sec.)		T_L	300	

Thermal Resistance Ratings

Parameter	Symbol	Typical	Maximum	Unit
Junction-to-Ambient	R_{thJA}		80	°C/W
Junction-to-Case	R_{thJC}		1.2	
Case-to-Sink	R_{thCS}	1.0		

Notes:
a. Duty cycle ≤ 1%

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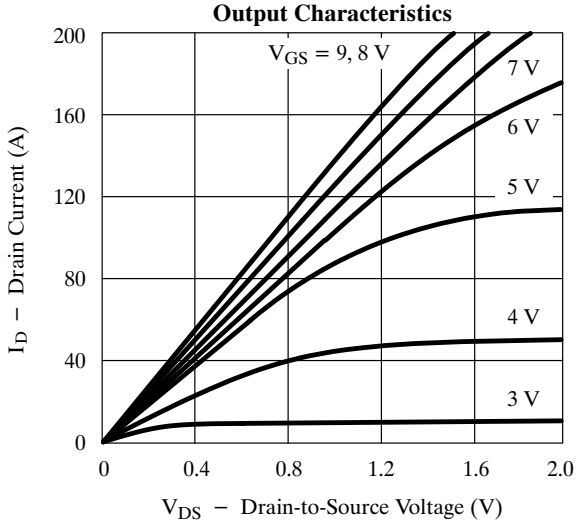
Specifications (T_J = 25°C Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ[a]	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 µA	30			V
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	0.8		3.0	
Gate-Body Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±500	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 24 V, V_{GS} = 0 V			25	µA
		V_{DS} = 24 V, V_{GS} = 0 V, T_J = 125°C			250	
On-State Drain Current[b]	$I_{D(on)}$	V_{DS} = 10 V, V_{GS} = 10 V	60			A
Drain-Source On-State Resistance[b]	$r_{DS(on)}$	V_{GS} = 10 V, I_D = 30 A		0.007	0.010	Ω
		V_{GS} = 5 V, I_D = 30 A		0.010	0.015	
		V_{GS} = 10 V, I_D = 30 A, T_J = 125°C		0.009	0.014	
Forward Transconductance[b]	g_{fs}	V_{DS} = 15 V, I_D = 30 A		45		S
Dynamic						
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		2600		pF
Output Capacitance	C_{oss}			1500		
Reverse Transfer Capacitance	C_{rss}			750		
Total Gate Charge[c]	Q_g	V_{DS} = 15 V, V_{GS} = 10 V, I_D = 60 A		100	120	nC
Gate-Source Charge[c]	Q_{gs}			10	15	
Gate-Drain Charge[c]	Q_{gd}			45	75	
Turn-On Delay Time[c]	$t_{d(on)}$	V_{DD} = 30 V, R_L = 1 Ω I_D ≃ 30 A, V_{GEN} = 10 V, R_G = 2.5 Ω		14	30	ns
Rise Time[c]	t_r			25	50	
Turn-Off Delay Time[c]	$t_{d(off)}$			65	100	
Fall Time[c]	t_f			45	80	
Source-Drain Diode Ratings and Characteristics (T_C = 25°C)						
Continuous Current	I_S				60	A
Pulsed Current	I_{SM}				240	
Forward Voltage[b]	V_{SD}	I_F = 60 A, V_{GS} = 0 V			1.6	V
Reverse Recovery Time	t_{rr}	I_F = 60 A, dI_F/dt = 100 A/µs		160		ns
Peak Reverse Recovery Current	$I_{RM(REC)}$			13		A
Reverse Recovery Charge	Q_{rr}			1.0		µC

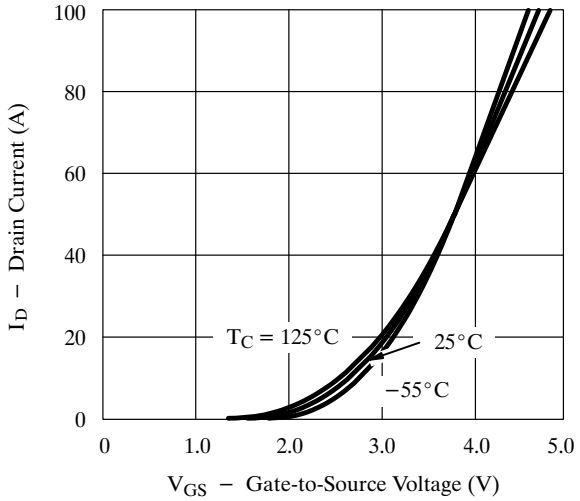
Notes:
a. For design aid only; not subject to production testing.
b. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2%.
c. Independent of operating temperature.

Typical Characteristics (25°C Unless Otherwise Noted)

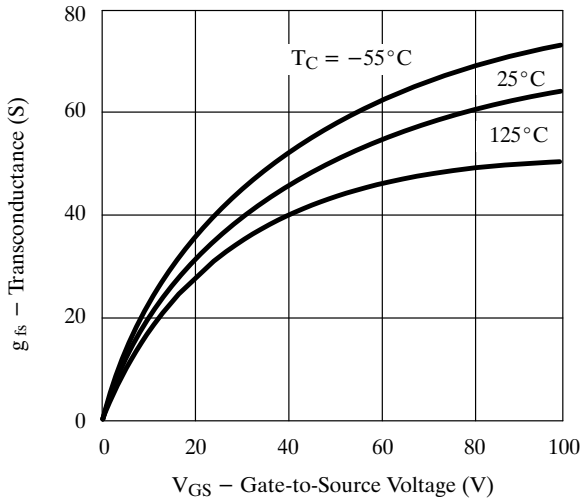
Output Characteristics



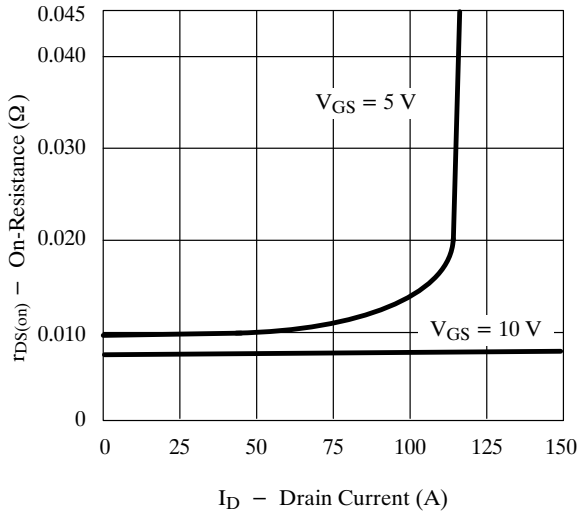
Transfer Characteristics



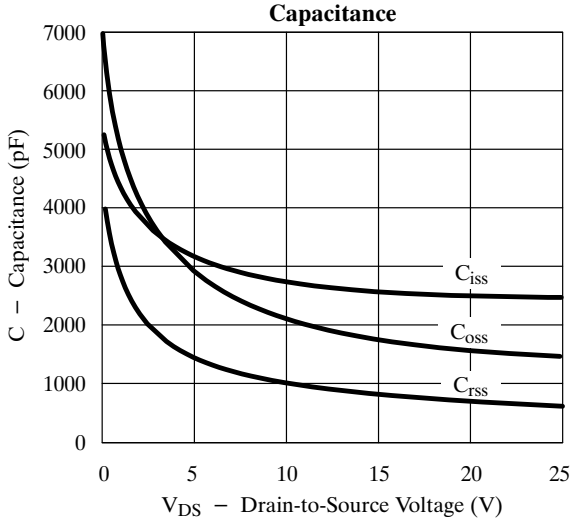
Transconductance



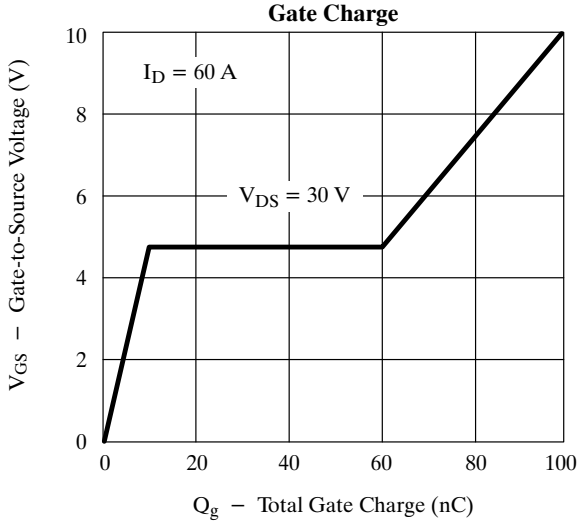
On-Resistance vs. Drain Current



Capacitance



Gate Charge



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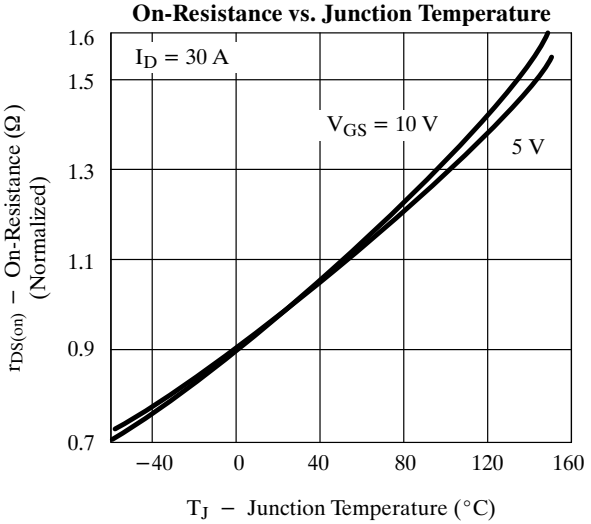
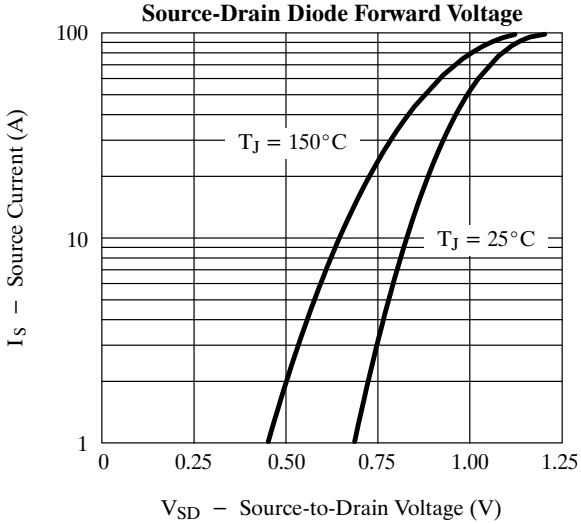
Typical Characteristics (25°C Unless Otherwise Noted)

On-Resistance vs. Junction Temperature

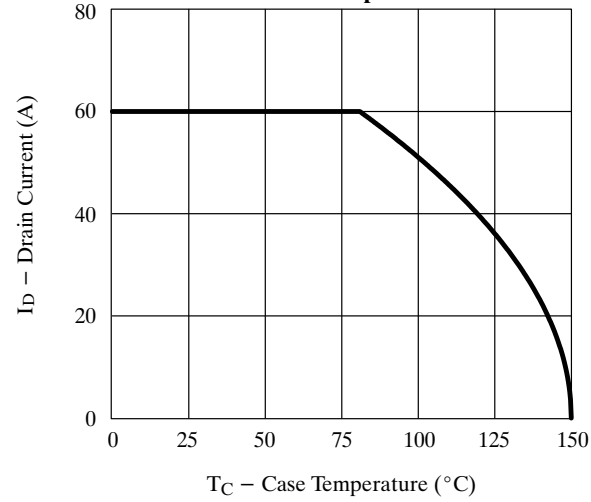


Source-Drain Diode Forward Voltage

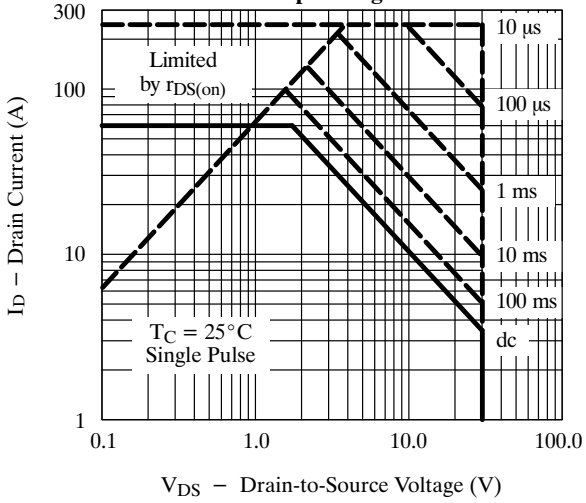


Thermal Ratings

Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case